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CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
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Claims 20-56, as of March 21, 2000 (*date response to first office action filed).*

Sub D1

20. (Once Amended) A method of fabricating a memory array, the method comprising the steps of:

forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein each access transistor includes, in order, a first source/drain region, a unitary body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor;

forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench;

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

21. The method of claim 20, wherein the step of forming a trench capacitor further includes the step of forming a second plate that surrounds the first plate.

22. The method of claim 20, and further comprising the step of forming a contact that couples a second plate of the trench capacitor to an underlying semiconductor layer.

23. The method of claim 20, where the step of forming a trench capacitor comprises the step of forming a second plate that forms a grid pattern in a layer of semiconductor material such that the grid surrounds each of the pillars that form the access transistors.

24. The method of claim 20, wherein the step of forming a trench capacitor comprises the step of depositing poly-silicon in crossing row and column isolation trenches formed around the pillars that define the access transistors.

25. A method of fabricating a memory array, the method comprising the steps of:

forming a first conductivity type first source/drain region layer on a substrate;

forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

forming a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array;

filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the access transistors on each column.

26. The method of claim 25, wherein the step of forming the first conductivity type source/drain region layer on the substrate comprises the step of forming the first conductivity type first source/drain region layer outwardly from the substrate to a distance sufficient for the first source/drain region layer to also function as a first plate of the capacitor for each memory cell in the array.

27. The method of claim 20, wherein the memory array comprises memory cells each occupying an area of $4F^2$, wherein F is a minimum feature size.

28. The method of claim 20, wherein the first source/drain region is N+ doped.

29. The method of claim 28, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

30. The method of claim 28, wherein the unitary body region is P- doped.

31. The method of claim 30, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

32. The method of claim 30, wherein the second source/drain region is N+ doped.

33. The method of claim 32, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

34. The method of claim 25, wherein the memory array comprises memory cells each occupying an area of $4F^2$, wherein F is a minimum feature size.

35. The method of claim 25, wherein the first source/drain region is N+ doped.

36. The method of claim 35, including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

37. The method of claim 35, wherein the unitary body region is P- doped.

38. The method of claim 37, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

39. The method of claim 37, wherein the second source/drain region is N+ doped.

40. The method of claim 39, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

41. A method of forming an array of memory cells upon a substrate, the method comprising:

forming a plurality of isolated vertical access transistors separated by trenches, comprising in order outward from the substrate, a first source drain region, a unitary body region, and a second source/drain region, wherein the separation of trenches is such that the area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

forming a trench capacitor for each memory cell, wherein a portion of the first source/drain region serves as a first plate of the capacitor;

forming two word lines in select trenches, with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming bit lines that interconnect select second source/drain regions.

42. The method of claim 41, wherein the first source/drain region is N+ doped.

43. The method of claim 41 including forming the first source/drain region to a thickness of approximately 3.5 micrometers.

44. The method of claim 42, wherein the unitary body region is P- doped.

45. The method of claim 43, including forming the unitary body region by epitaxial growth of single-crystalline P- silicon to a thickness of approximately 0.5 microns.

46. The method of claim 44, wherein the second source/drain region is N+ doped.

47. The method of claim 46, including forming the second source/drain region by implanting the N+ dopant to a depth of approximately 0.1 microns.

48. The method of claim 41, wherein forming the trench capacitor further includes the step for forming a second plate that surrounds the first plate.

49. A method of forming an array of memory cells on a substrate, the method comprising:

forming atop the substrate a first layer of a first conductivity type of single crystalline silicon, a second layer of a second conductivity type of single crystalline silicon, and a third layer of the first type of single crystalline silicon;

selectively etching through the third through first layers and partially into the substrate so as to form a plurality of trenches and pillars spaced apart such that the surface area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

filling the trenches with a conductive material so as to provide for a common plate for capacitors associated with each memory cell, such that a portion of the first layer in each pillar serves as a plate for the capacitor;

electrically interconnecting select pillars by word lines electrically coupled to the second

layer of the select pillars;

electrically interconnecting the select pillars by bit lines electrically coupled to the third layer of the select pillars.

50. A method according to claim 46, wherein the first conductivity type is N+ and the second conductivity type is P-.

51. A method of fabricating an array of memory cells on substrate, the method comprising:

forming spaced apart access transistors isolated by trenches, each access transistor comprising in order from the substrate outward, an N+ - doped first source/drain region, a P- doped body region and an N+ -doped second source/drain region;

forming capacitors in the trench corresponding to each access transistor, wherein a portion of the N+ -doped first source/drain region adjacent the substrate serves as a plate for the capacitor corresponding to each access transistor; and

electrically connecting the access transistors in a manner that allows for an electrical charge to be accessed or stored in each capacitor via the corresponding transistor.

52. A method according to claim 51, wherein electrically connecting the access transistors includes:

forming a number of word lines in a number of trenches , wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

53. A method of forming a memory device having an array of memory cells and a minimum feature size F, comprising:

forming a plurality of vertical access transistors separated by trenches and laid out in a substantially checker-board pattern such that the memory cells occupy an area of $4F^2$, wherein the formation of the vertical access transistors consists of the steps forming a first source/drain region of a first dopant type, forming a body region of a second dopant type atop the first source/drain region, and forming a second source/drain region of a second dopant type atop the body region;

forming a capacitor in the trenches by lining the trench with a gate oxide and then filling the trench with polysilicon of the first type so as to surround a portion of the first source/drain region such that the surrounded portion of the first source/drain region serves as a first plate of the capacitor and the polysilicon in the trench serves as a second plate of the capacitor; and

electrically connecting the transistors via bit lines and word lines so as to provide the capability of accessing a charge stored in one or more of the capacitors or providing a charge thereto.

54. The method of claim 53, further including connecting the word lines to a word line decoder and the bit lines to a bit line decoder to provide selective access to the memory cells.

55. A method of forming an electronic device having an array of memory cells and a minimum feature size F, comprising:

forming on a substrate a plurality of spaced apart access transistors each comprising in order outward from the substrate, a first layer of N+ dopant serving as first source/drain, a second layer of P- dopant serving as a body region and a third layer of N+ dopant serving as a second source/drain region;

wherein the forming of the access transistors includes the step of forming trenches therebetween so as to provide a memory cell area of $4F^2$;

forming, for each transistor, a capacitor in the trenches by filling the trench with a thin layer of oxide and polysilicon such that a portion of the first source/drain, the oxide layer and the

polysilicon respectively serve as a first plate, a dielectric, and a second plate for the capacitor

electrically connecting the transistors with word lines and bit lines;

connecting the word lines to a word line decoder;

connecting the bit lines to a bit line decoder;

operatively connecting the word line and bit line decoders to an address buffer; and

interfacing the address buffer to an electronic system via address lines.

56. The method of claim 55, wherein the electronic system is a microprocessor.